CX-40 Cortex-M4 Dev Board

CRL-CX40-DEV

120 MHz ARM® Cortex®-M4F development board with USB-C, castellated edge I/O and a pre-flashed bootloader — a 52 × 25 mm module for prototyping and drop-in production.

1 KEY FEATURES

- ARM Cortex-M4F core @ 120 MHz, single-cycle FPU + DSP
- 512 KB Flash, 128 KB SRAM (16 KB retention in Stop mode)
- 48 GPIO on 0.05" castellated edges, all 5 V-tolerant except PA0–PA3
- USB-C for power, programming and USB 2.0 Full-Speed device
- Two I²C, three SPI, four UART, 2× 12-bit ADC (1 MSPS), 2× DAC
- Pre-flashed UF2 bootloader; SWD header for JTAG/SWD debug
- Onboard 3.3 V / 800 mA LDO; VIN 4.5–5.5 V via USB-C or VIN pad

2 ORDERING & COMPLIANCE

Order code	CRL-CX40-DEV
Maker	CORELIC
Packaging	Antistatic clamshell, 1 pc
MSL	Level 3 (module), 168 h floor life
Weight	7.4 g
RoHS 3 / REACH	Compliant (see DoC DoC-CRL-CX40-DEV)

RoHS 3 · REACH · CE · FCC Part 15B

3 ABSOLUTE MAXIMUM RATINGS

PARAMETER	MIN	MAX
VIN (USB-C / VIN pad)	-0.3 V	6.0 V
3V3 rail sink/source	—	800 mA
GPIO source/sink per pin	—	±20 mA
Storage temperature	-40 °C	+105 °C
ESD (HBM, all pins)	—	±4 kV

Stresses beyond these ratings may cause permanent damage. Operation at maximum ratings for extended periods is not recommended.

4 ELECTRICAL CHARACTERISTICS

V_{IN} = 5.0 V, T_A = 25 °C unless noted.

SYMBOL	PARAMETER	TYP
V_{DD}	Operating voltage	3.3 V
I_{RUN}	Run @120 MHz, all peripherals	42 mA
I_{SLEEP}	Sleep (WFI, 120 MHz clock)	9.8 mA
I_{STOP}	Stop mode, RTC on	18 µA
I_{STBY}	Standby, RAM retention	2.4 µA
t_{WAKE}	Stop → Run wake time	6 µs
V_{IH}	Input high threshold	2.0 V
$f_{I²C}$	I²C bus, Fast-mode Plus	1 MHz
f_{SPI}	SPI master clock	30 MHz

5 OPERATING CONDITIONS

Operating temperature	-40 °C to +85 °C (industrial)
Humidity	10–90 % RH, non-condensing
Clock source	24 MHz crystal + internal PLL
Reflow (module)	245 °C peak, ≤ 30 s, per J-STD-020

6 BOOTLOADER & DEBUG

Double-tap **RESET** to enter the UF2 bootloader — the board mounts as a USB drive **CX40BOOT**. Drag a `.uf2` to flash. Factory UART console is on **PA9 (TX) / PA10 (RX)** at **115200 8N1**. SWD debug on the 4-pin SWD header (SWCLK/SWDIO/GND/3V3).

7 EDGE CONNECTOR PIN MAP (SELECTED)

PIN	DEFAULT FUNCTION	ALT FUNCTIONS	NOTES
`PA0`	ADC1_IN0	TIM2_CH1 / UART4_TX	Not 5 V-tolerant
`PA9`	UART1_TX	I2C1_SCL / TIM1_CH2	Bootloader console TX
`PA10`	UART1_RX	I2C1_SDA / TIM1_CH3	Bootloader console RX
`PB6`	I2C1_SCL	UART1_TX / TIM4_CH1	Fast-mode Plus, 4.7 kΩ pull-up onboard
`PB7`	I2C1_SDA	UART1_RX / TIM4_CH2	Fast-mode Plus, 4.7 kΩ pull-up onboard
`PB13`	SPI2_SCK	TIM1_CH1N / CAN2_TX	30 MHz max

PIN	DEFAULT FUNCTION	ALT FUNCTIONS	NOTES
PC13	USER_LED	GPIO	Active-low onboard LED
VIN	5 V input	—	Diode-OR with USB-C VBUS

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